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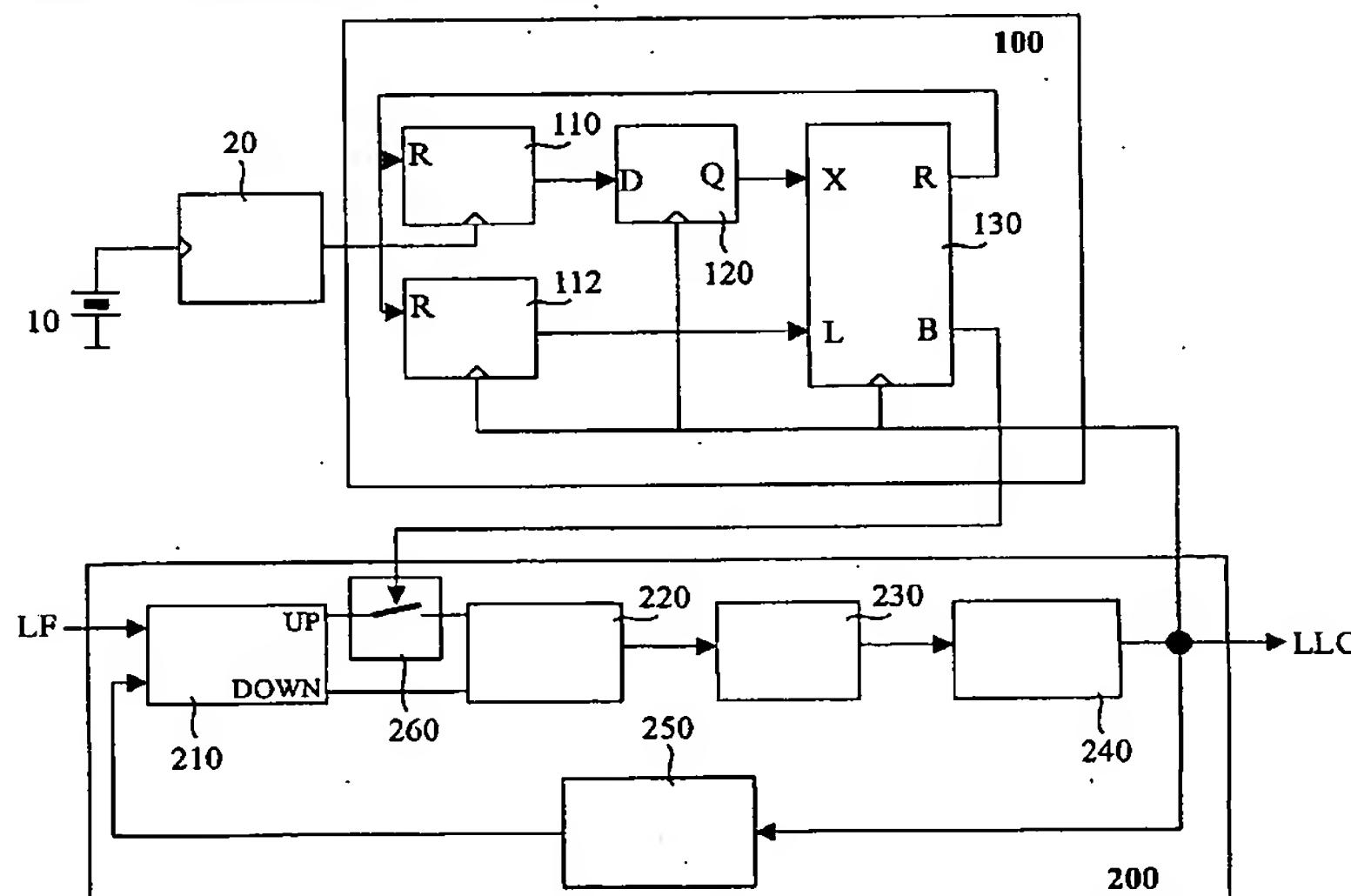
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(54) Title: PLL CIRCUIT



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(57) Abstract: The present invention relates to a phase locked loop arrangement having an oscillator circuit (240) controlled in response to an output signal of a phase or frequency detection circuit (210), wherein change control means (130) are provided for generating a blocking signal in response to the outputs of a first timer means (110) to which a predetermined threshold frequency is supplied and a second timer means (112) to which an output frequency of the oscillator circuit (240) is supplied. Based on the blocking signal, blocking means (260) suppress supply of the output signal to said oscillator circuit (240). Thereby, the output frequency of the PLL arrangement can be prevented from changing beyond the frequency threshold, while only one PLL circuit is required.



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